

CRAY T3E System



NATIONAL PARTNERSHIP FOR ADVANCED COMPUTATIONAL INFRASTRUCTURE

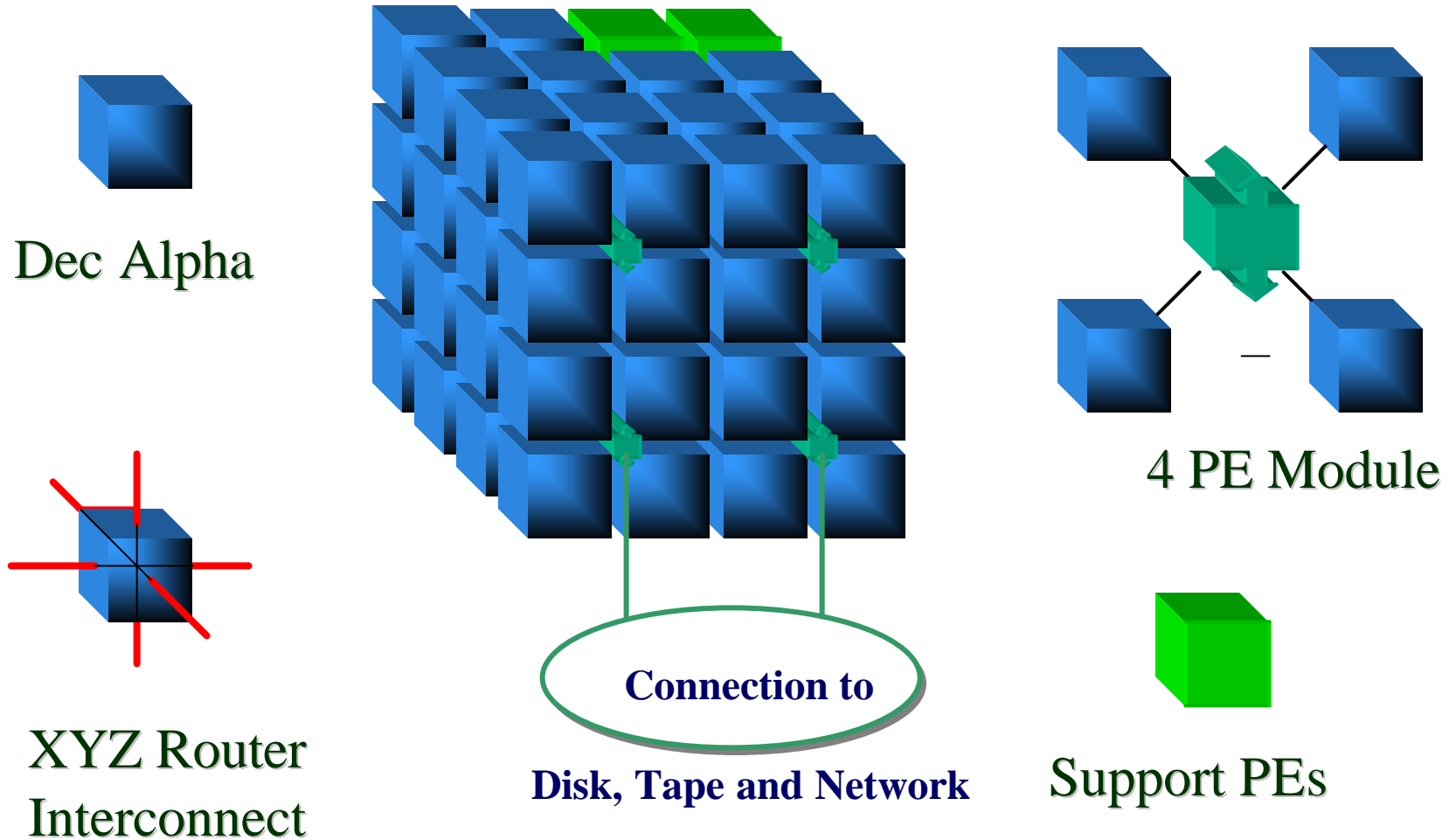
Hardware overview-16

NAVAL OCEANOGRAPHIC OFFICE MAJOR SHARED RESOURCE CENTER

CRAY T3E

- 300 Mhz (peak : 600 MFLOPS), 450 Mhz (peak : 900 MFLOPS), and 600 Mhz (peak : 1200 MFLOPS)
- Each processor is DEC Alpha 21164 chip
- Memory sizes provided :
 - T3E-1200 : 256MB to 2048 MB
 - T3E-900 : 64 MB to 2048 MB (NAVO 544 PE, 256MB/PE)
 - T3E-600 : 64 MB to 2048 MB
- 3D torus interconnect

T3E Structure



Processor

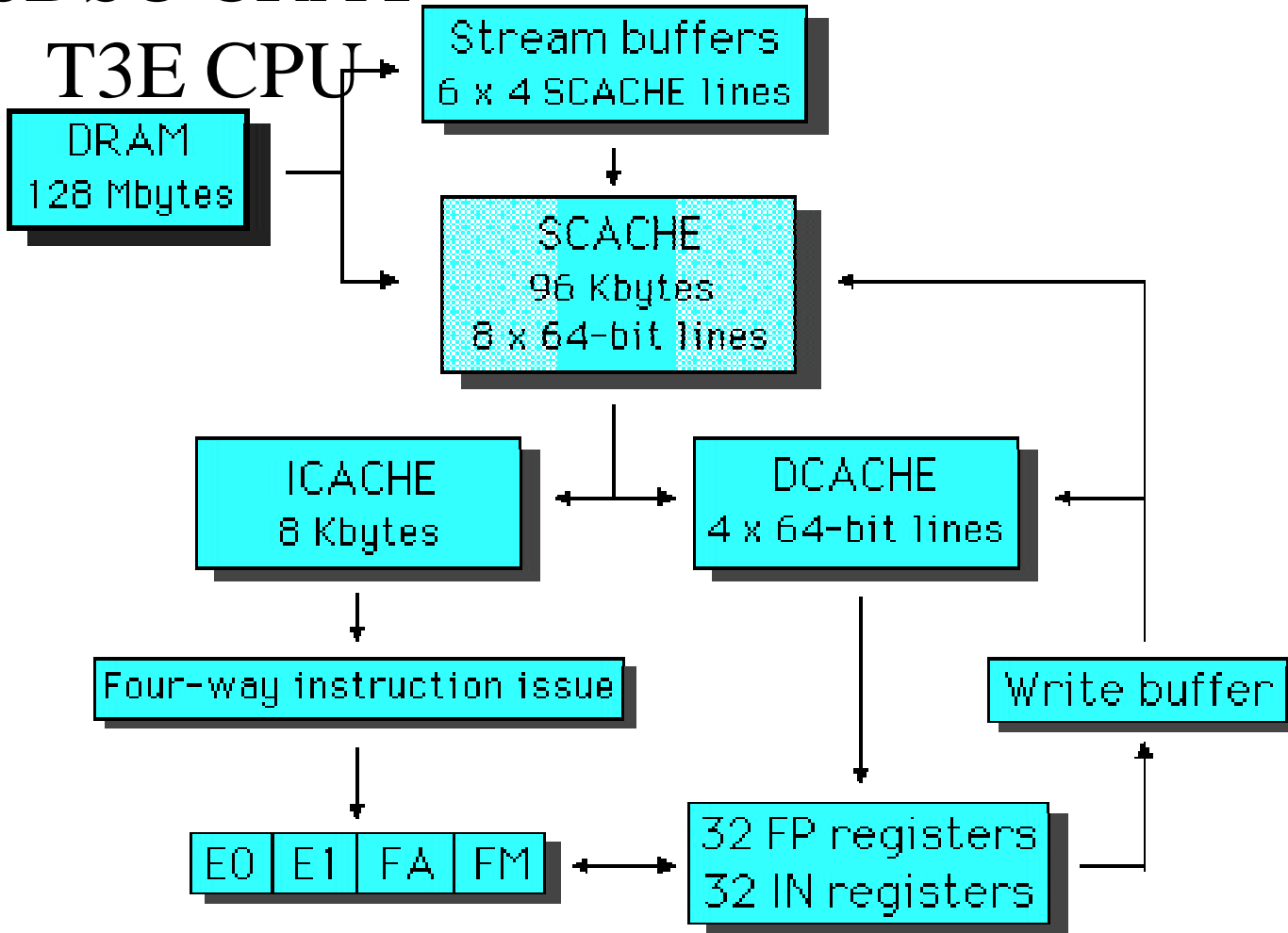
- CRAY T3E:
 - DEC 21164 processor (also called EV-5)
 - Superscalar - issues up to 4 instructions/CP
 - 2 float (1 add, 1 multiply) and 2 integer (includes 2 loads or 1 store)
 - On chip 8 KB direct mapped data cache (DCACHE)
 - On chip 8 KB direct mapped instruction cache (ICACHE)
 - On chip 96 KB 3-way set associative secondary cache (SCACHE)

Floating Point Execution Unit

- The Floating Point Execution Unit (FPU) contains:
 - 32 64-bit IEEE floating point registers
 - a fully pipelined floating point multiply unit (4 CP latency)
 - a fully pipelined floating point add unit (4 CP latency)
 - a non-pipelined floating point divide unit (15-31 CP latency for 32-bit FP divide, 22-61 CP latency for 64 bit divide) and shares hardware with FP add unit

SDSC CRAY

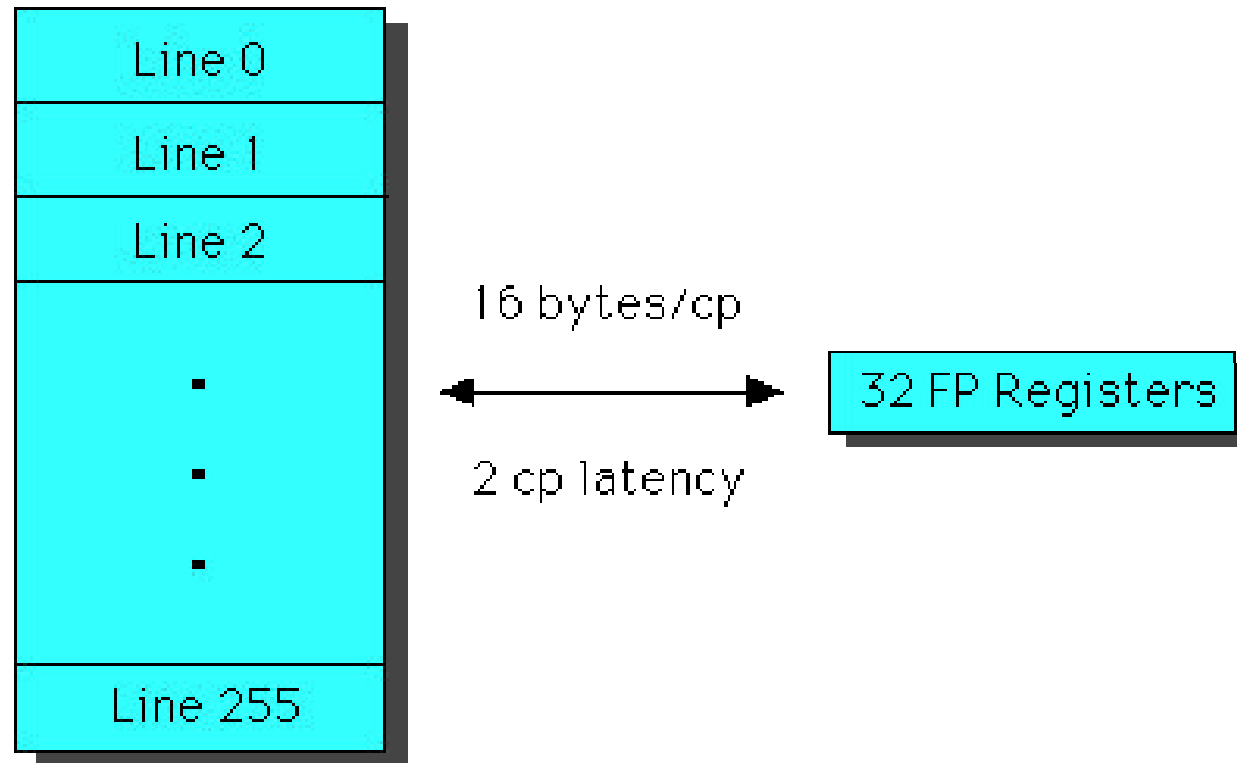
T3E CPU



DCACHE

- On-chip data cache (L1 cache)
- 8 Kbytes direct-mapped
- Divided into 256 lines, each line is 32 Bytes or 4 words per line

DCACHE

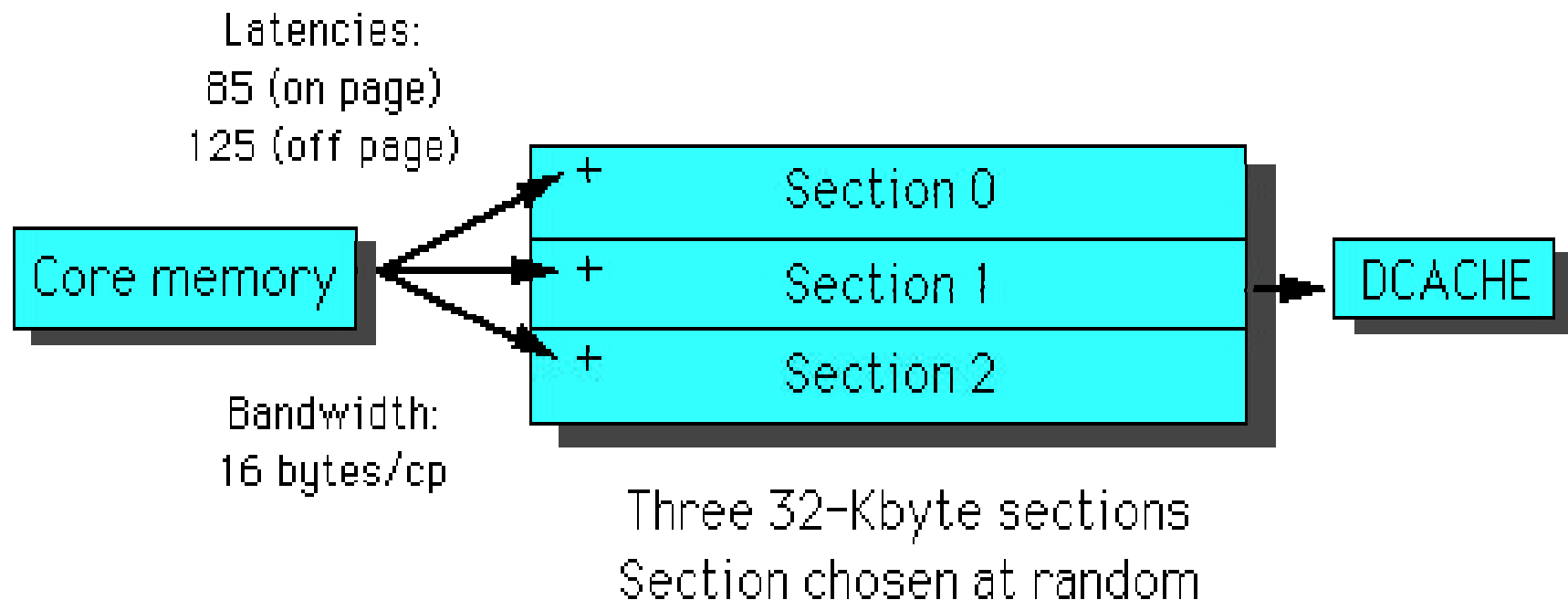


Four doubles per line
(32 bytes)

SCACHE

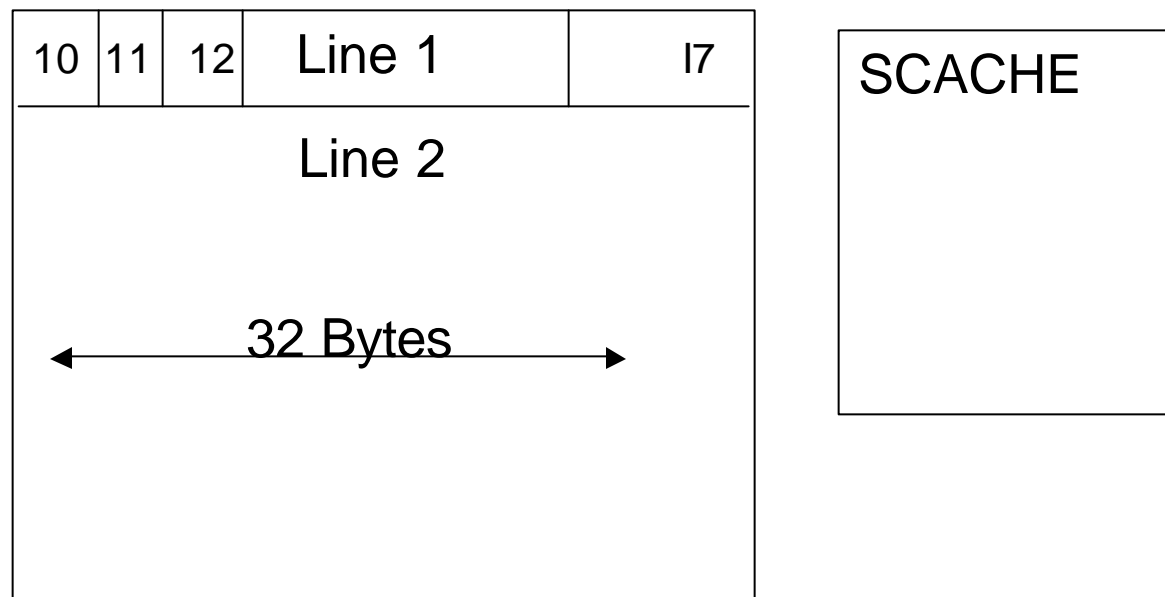
- On-chip secondary cache (L2 cache)
- Three-way set associative
- 96 Kbytes (3 X 32 KBytes)
- 1536 lines with eight words per line
- Cache replacement: Random replacement

SCACHE



Instruction Cache (ICACHE)

- 8 KB, direct mapped
- Can hold upto 2000 instructions (1 instruction = 4 B)
- 255 Lines



Memory Characteristics of T3E

Cache access	Latency	Bandwidth
L1 cache load	6.67 ns - 2CP/load	4.8 GB/sec (2 words/CP)
L2 cache load	26.67 ns - 8CP/load	4.8 GB/sec (2 words/CP)

Interconnect Network and I/O

- 3 Dimensional Torus Network
- Torus links provide a raw bandwidth of 600 MB/s in each direction and payload bandwidths ranging from 100 to 480 MB/s
- 3-D torus allows $n/2$ "hop" communication between any two nodes (where n is number of nodes in either x, y, or z direction)
- I/O: The scalable GigaRing channel, a counter-rotating, dual-ring channel can deliver peak of upto 1 Gbytes/s

Latency and Bandwidth of T3E600 Network

Library	Network latency (micro sec)	Bandwidth (MB/Sec)
Shmem	1	350
PVM	11	150
MPI	14	260

Peak: T3E600 : 500MB/s; T3E900: 500MB/s; T3E1200 : 650MB/s

Advanced Features of T3E

- Stream buffers
 - Allows prefetching from DRAM to Streams
 - Automatically hardware-managed
- E-registers
 - Special hardware that allows to by-pass cache
 - Allows to load data directly from memory to registers
- CRAY's T3E web page :

<http://www.cray.com/products/systems/crayt3e>



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